DOCUMENT:	**PROPOSAL ABSTRACT**
AGENCY:	DARPA/TTO
PROGRAM:	Power Aware Computing and Communications (PAC/C)
BAA:	99-37
PROGRAM POC:	Dr. Jose Munoz *fx*: 703-522-7161

TECHNICAL TOPIC AREAS: Architectural approaches, algorithms, middleware, and benchmarks/ simulations, for optimally exploiting certain innovative circuit designs and for dynamic voltage/frequency scaling.

TITLE: **Dynamic Optimization of Semi-Adiabatic Power-Managed Architectures**

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PERFORMANCE PERIOD: 1 May 2000 - 30 Apr 2002 (24 months)
COST SUMMARY:

TOTAL BASE COST:	$1,048,624
YEAR 1 COST:	$ 551,543
YEAR 2 COST:	$ 497,081
COST SHARING:	$ 0
OPTIONS:	None.

BUSINESS TYPE: **OTHER EDUCATIONAL**

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A. Innovative Claims

Conventional CMOS digital circuits dissipate all of the energy stored on a logic circuit node to heat every time the node's bit value is changed. In contrast, adiabatic circuits recycle most of the signal energy and reuse it on subsequent cycles to represent other information. Previous research [1] has shown that when operating in very low-power regimes (e.g., 100 to 1000X less than conventional circuits), thoroughly adiabatic circuits (such as described in [2,3]) provide better power/performance scaling for computation than any possible non-adiabatic approach. We propose novel component architectures, control techniques, and system design methodologies that would optimally or near-optimally exploit the improved power scalability of adiabatic systems, in the context of a complete, dynamically power-managed computing and communications system.

In medium-to-high power regimes (1 to 10X less power than conventional circuits), adiabatic circuits, due to higher overheads, may be less efficient than more traditional power reduction approaches. In order to enable dynamically optimized system performance over all power levels in diverse applications, we propose a novel dual-module component architecture in which a given IC component's functionality would be implemented redundantly in both adiabatic and non-adiabatic forms by distinct hardware modules, only one of which would be powered at a given time.

Associated device-control software would dynamically select which hardware module to operate, based on a best-performance model constrained by previously-gathered benchmarks and simulations, and by a run-time estimate of currently-available power. Additionally, the software would dynamically adjust the selected module's clock speed and power supply voltage, within hardware tolerances, to maximize performance within dynamic power constraints.

This device-control software would operate in the context of middleware or OS-level support for integrated power management for the entire application unit (e.g., desktop, handheld, standoff, airborne, or spaceborne unit). We envision a generally-applicable ACPI-like power management approach, in which every electronic component would eventually interface to a system-wide power management communication and control network. ACPI itself would require enhancements before it could support sophisticated allocation of power in order to optimize global system performance at a more flexible range of power levels (beyond just off, on, and sleep). Such enhancements could be developed in parallel by other groups, or investigated in a follow-on effort to this proposal.

Further, the proposed dual-module (adiabatic/non-adiabatic) architecture represents only one available design option. For sufficiently paralellizable applications, our previous research suggests that an alternative fully adiabatic architecture would be superior [1]. When total available power P is relatively high, if the required computation can be implemented in parallel, then one option is to simply divide P among many concurrent functional units, each of which operates in a low-power regime. We thus propose to leverage the smaller minimum energy per operation of the adiabatic approach to achieve greater total performance within a given power budget, at the cost of increased hardware required for a parallel implementation.

The proposed system design methodology would systematically compare the merits of a (1) semi-adiabatic approach, (2) fully adiabatic, highly-parallelized approach, and (3) a traditional non-adiabatic approach, thus ensuring comprehensive optimization. System design and analysis constraints would include but not be limited to hardware component costs, the range of power levels to be supported, the degree to which an application could be computed in parallel, and the utility of increased component performance in the given application. Software tools would be developed for simulation and benchmarking to support this system design decision process.

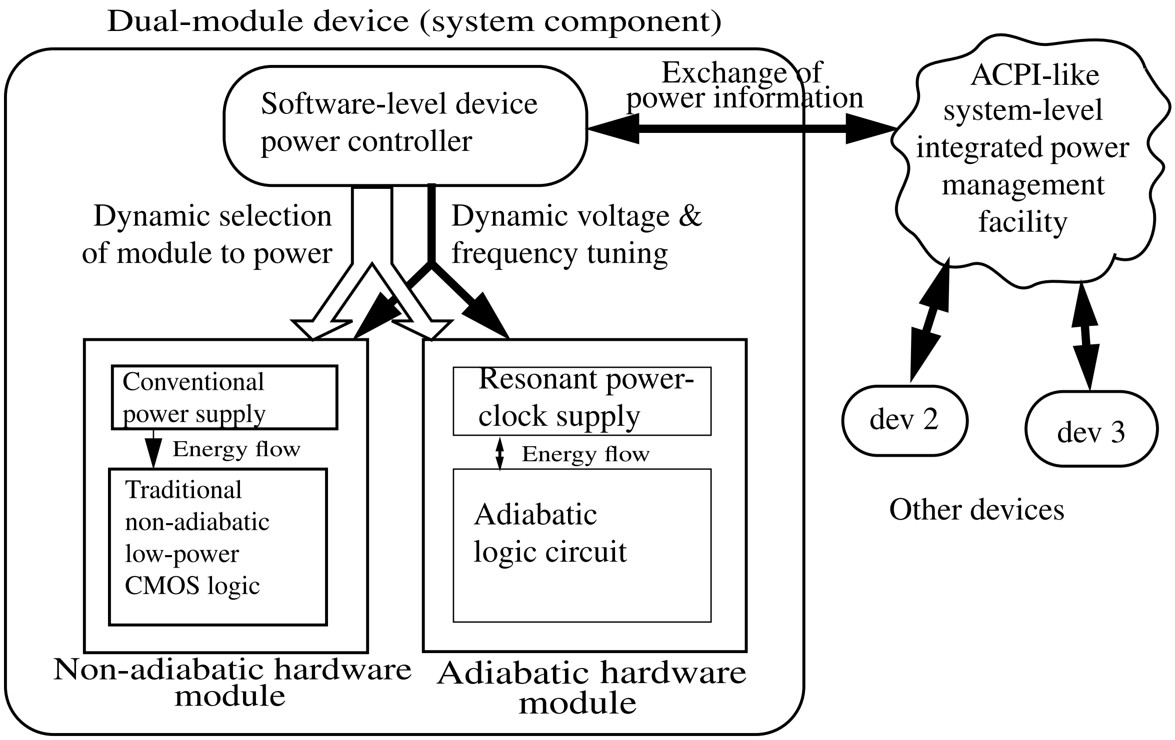

Figure 1. Semi-adiabatic dual-module device architecture.

B. Technical Rationale, Approach, and Plan.

B.1. Technical Rationale. Based on our reading of the BAA, a key goal of the Power Aware Computing and Communication (PAC/C) program is the development of effective techniques for building complete software and hardware systems that perform as efficiently as possible at run-time, given realistic and varying environmental and application-specific constraints on power.

Adiabatic technology now exists as an available option for low-power computing [2,6]. Its power/performance ratio scales differently than in other technologies; this becomes advantageous at sufficiently low power levels. The precise tradeoffs between cost, power consumption, speed, voltage, and choice of technology are still being elucidated as adiabatic technology evolves [1,7].

Because of the difference in scaling properties, neither adiabatic nor non-adiabatic technology can alone provide optimal performance at a wide range of available power levels. We therefore propose to investigate the hybrid approach described in the Innovative Claims section and illustrated in Figure 1 above.

Our proposed approach significantly addresses many of the PAC/C concerns with regards to providing integrated, multi-technology, software/hardware system-level solutions and tools to support them. Our proposal emphasizes the choice of circuit-level technologies and operating parameters. However, once the tools for analyzing the circuit-level tradeoffs have been developed, they can then be integrated with tools for optimizing systems along other dimensions (algorithm design, network architecture, etc.) to produce a next generation of highly sophisticated tools that would simultaneously optimize a custom system's design along many dimensions, to produce a globally optimal or near-optimal solution. Such integration of tools would be a good target for a further two-year follow-on effort.

B.2. Technical Approach. We propose a four-phase approach for this study, namely:

Phase 1. **Preliminary data collection.** Acquire required equipment, recruit supporting personnel, then design and fabricate preliminary hardware to collect experimental results on power/performance of traditional and simple adiabatic designs such as those studied in our earlier research at MIT [1,2,3]. To achieve comparability, all tested circuits would implement identical functional behavior - one or more realistic algorithms of interest to the sponsor. The results of Phase 1 experiments are expected to confirm the results of earlier experiments [2, 5] in a more accurate and detailed form.

Phase 2. **Model refinement and tool-building.** Given the results of Phase 1, we expect to confirm and refine our existing mathematical models for evaluating design tradeoffs between speed, power, voltage, adiabatic versus non-adiabatic design, etc. In particular, we expect to accurately characterize the power threshold below which adiabatic technology becomes advantageous. We also expect to verify our predictions that a highly parallel adiabatic design can produce a significantly greater throughput per Watt than the alternatives, albeit with a higher transistor count. We would embody our models in new software tools that would permit easy estimation of the power/performance profile of adiabatic and non-adiabatic versions of any new component being designed.

Phase 3. **Demonstration system.** Following preliminary experiments and analysis (Phases 1 and 2), we propose to develop a demonstration system. This would be comprised of an integrated, multi-technology, dynamically power-managed component, which would contain submodules implementing two or more low-power approaches. Signals from a control system (running in software on an external processor) would dynamically switch between functional modules, adjusting their parameters at runtime per available power. The precise control strategy would be based on the finely-tuned models developed in Phase 2.

Phase 4. **Final testing, assessment, and delivery.** Testing of the proposed power-managing, self-optimized hardware/software components is expected to show that across all power levels, the semi-adiabatic component's performance closely matches the estimated optimum performance predicted from the models developed in Phase 2. The complete demonstration system (hardware designs & software tools) would be documented, together with results and a final report, and would be packaged and delivered to industry partners and the public domain.

B.3. Constructive Plan. The proposed performance period is 24 months, from 1 May 2000 through 30 Apr 2002. The proposed schedule of work is elaborated below to the subtask level. The dates of tasks overlap. The full proposal would also specify milestones and subtask dates.

Task 1. **Metrology & benchmarking.** Acquire test equipment and develop design, analysis, and test requirements. *1 May 2000 - 31 Oct 2000 (6 months)*

ST1.1. Acquire research equipment and test to verify functionality: Components for resonant power supplies, electronic test equipment not available in-house, calorimetry apparatus to verify power consumption, and CAD circuit design tools.

ST1.2. Develop requirements for application functionality and testing of hardware components. Design benchmarks for power/performance characterization.

ST1.3. Build and test resonant power waveform generators suitable for driving very low-power adiabatic systems, using advanced techniques such as described in [4], or even newer techniques currently being developed.

ST1.4. Design, fabricate (MOSIS), and test functionality and power of very simple circuits to validate the design cycle, using measurement techniques such as described in [5].

Task 2. **Demonstration system.** Design and develop preliminary and final real hardware ICs to provide data for modeling and to demonstrate the efficiency of the final integrated approach. *1 Jun 2000 - 31 Oct 2001 (17 months)*

ST2.1. Based on the requirements developed in ST1.2, design, fabricate and test separate prototype conventional and adiabatic hardware components implementing the chosen application functionality. Data on these components would be used to refine tradeoffs.

ST2.2. Based on results of testing of prototype circuits, design demonstration components implementing the application functionality, and integrate them into a single dual-technology component.

ST2.3. Test integrated component under a range of conditions, first under manual control of parameters, then using the software device controller that would have been concurrently developed in ST4.2 (below).

Task 3. **Modeling and Optimization.** Refine models of low-power circuits, methods for optimizing circuit performance and choosing the best technology, and techniques for simulating power consumption behavior. *1 Sep 2000 - 31 Apr 2001 (8 months)*

ST3.1. Based on results from ST1.3, enhance our power vs. frequency/voltage models of adiabatic power supplies.

ST3.2. Based on results from ST1.4, enhance our existing models of low-power logic circuits, to produce realistic performance estimates of adiabatic versus non-adiabatic low-power computing technology at a wide range of parameter settings.

ST3.3. Using results of testing of prototype circuits from ST2.1, refine analytical techniques [1] for comparing tradeoffs of various adiabatic/non-adiabatic architectures.

ST3.4. Design run-time dynamic optimization algorithms for selecting between adiabatic or non-adiabatic technology, and for selecting optimal values of adjustable parameters.

Task 4. **Software development.** Develop & test key software, including analytical component design and simulation tools, and run-time device drivers for dynamic optimization.
1 Mar 2001 - 31 Dec 2001 (10 months)

ST4.1. Develop and test analytical tools for design-time determination of the best circuit technologies to use for a given component, subject to the requirements of a particular custom application system.

ST4.2. Using results of ST3.4, develop and test run-time control software (device driver) for dynamically selecting between alternative modules and adjusting power/frequency parameters so as to achieve optimal performance under varying power constraints.

ST4.2. Further refine software of ST4.1 and ST4.2 based on results of testing of the integrated system from ST2.3.

Task 5. **Technology transfer.** Final packaging, documentation & delivery of key results, models, designs, and software to partners (see below) in defense and industry.
1 Jan 2002 - 30 Apr 2002 (4 months)

The above schedule is more densely filled early in the performance period, and more sparsely filled later. This provides room for accomodating any unanticipated delays.

Personnel Assignment. As PI, Dr. Frank would supervise and coordinate the project. Additionally, as an expert in adiabatic circuits, Dr. Frank would contribute to many aspects of the adiabatic logic design of the demonstration hardware. Dr. Frank is also interested in performing detailed power measurements, modeling tradeoffs, and designing the various software components. Dr.

Schmalz, an expert in parallel systems and image-processing algorithms, would select the application functionality and design our parallel implementations. Dr. Ngo, a power supply expert, would be in charge of the design, characterization, and optimization of conventional and adiabatic power supplies. Dr. Fox would assist with circuit modeling and analysis. Dr Lee, an expert in embedded and real-time systems, would work on software components. Dr. Eisenstadt would be in charge of the development of the detailed VLSI design and layout. Finally, Dr. O would assist in transistor-level modeling and any mixed-signal (analog + digital) aspects of the design.

Technology Transfer. Many of Dr. Frank's MIT colleagues in adiabatic circuits have gone on to work in industry, such as Saed Younis at Qualcomm, and Carlin Vieri and Josie Ammer at Microdisplay. These are promising contacts for initiating technology transfer pathways for the application of new low-power techniques in the areas of wireless communications and embedded systems. In 1997, Dr. Frank was himself offered a position in Texas Instruments' DSP research group, which offers another promising deployment pathway. Frank also knows Darshan Patra at Intel, who has done adiabatic work. Finally, CISE's many partners on its Industry Advisory Board offer still more opportunities for early, close industry collaboration throughout this project.

C. Comparison with other ongoing research

The only major current competing program in adiabatic circuits of which we are presently aware is the ACMOS group of Athas et al. at USC's Information Sciences Institute [6,7]. ISI's work is of high quality, and the MIT group has worked with them on several occasions. However, ISI's focus tends to be the evolutionary, incremental application of adiabatic techniques within only selected portions of a processor - such as its buses or pad drivers only - which limits the energy efficiency that can be attained, since the energy of non-adiabatic portions comes to dominate. In contrast, the more thorough MIT/UF approach offers better power/performance scaling, lower minimum energy, and now, best performance at all power levels in this multi-technology proposal.

D. References

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[7] W.C. Athas, L."J." Svensson, J.G. Koller, N. Tzartzanis, E. Chou, Low-Power Digital Systems Based on Adiabatic-Switching Principles, in the IEEE Transactions on VLSI Systems, pp 398-407, Dec. 1994. Also see http://www.isi.edu/acmos/acmosPapers.html